

- ◆ Structure Silicon monolithic integrated circuit
- ◆ Product Single Channel 16-bit CIS/CCD Analog Front End
- ◆ Type **BU6574FV**
- ◆ Features
 - Correlated double sampling (CDS)
 - Programmable gain amplifier (8bit resolution)
 - 16bit 6MSPS ADC
 - Serial control interface
 - Offset calibration DAC (8bit resolution)
 - Internally generated voltage references
 - 4bit wide multiplexed data output format

◆ Absolute maximum ratings (Ta=25°C)

| Parameter | Symbol | Ratings | Unit |
|---------------------------|--------------------|----------------------------------|------|
| Supply voltage 1 | V _{AVDD} | -0.2 to 4.0 | V |
| Supply voltage 2 | V _{DVDD} | -0.2 to 4.0 | V |
| I/O supply voltage | V _{VDDIO} | -0.2 to 4.0 | V |
| Digital input voltage *1 | V _{ID} | -0.2 to V _{VDDIO} + 0.3 | V |
| Digital output voltage *2 | V _{OD} | -0.2 to V _{VDDIO} + 0.3 | V |
| Analog input voltage *3 | V _{IA} | -0.2 to V _{AVDD} + 0.3 | V |
| Analog output voltage *4 | V _{OA} | -0.2 to V _{AVDD} + 0.3 | V |
| Storage temperature | T _{stg} | -25 to 125 | °C |
| Power dissipation *5 | P _d | 400 | mW |

*1 : Pin No.3,4,6,8,9 *2 : Pin No.10,11,12,13 *3 : Pin No.20 *4 : Pin No.16,17,18,19
 *5 : Reduced by 4mW for each increase in Ta of 1°C over 25°C

◆ Operating conditions (Ta = 0°C to 70°C)

| Parameter | Symbol | MIN | TYP | MAX | Unit |
|--------------------|--------------------|-------|-----|-------|------|
| Supply voltage 1 | V _{AVDD} | 3.135 | 3.3 | 3.465 | V |
| Supply voltage 2 | V _{DVDD} | 3.135 | 3.3 | 3.465 | V |
| I/O supply voltage | V _{VDDIO} | 3.0 | 3.3 | 3.6 | V |

This product is not designed for protection against radioactive rays

Status of this document

The Japanese version of this document is the formal specification.

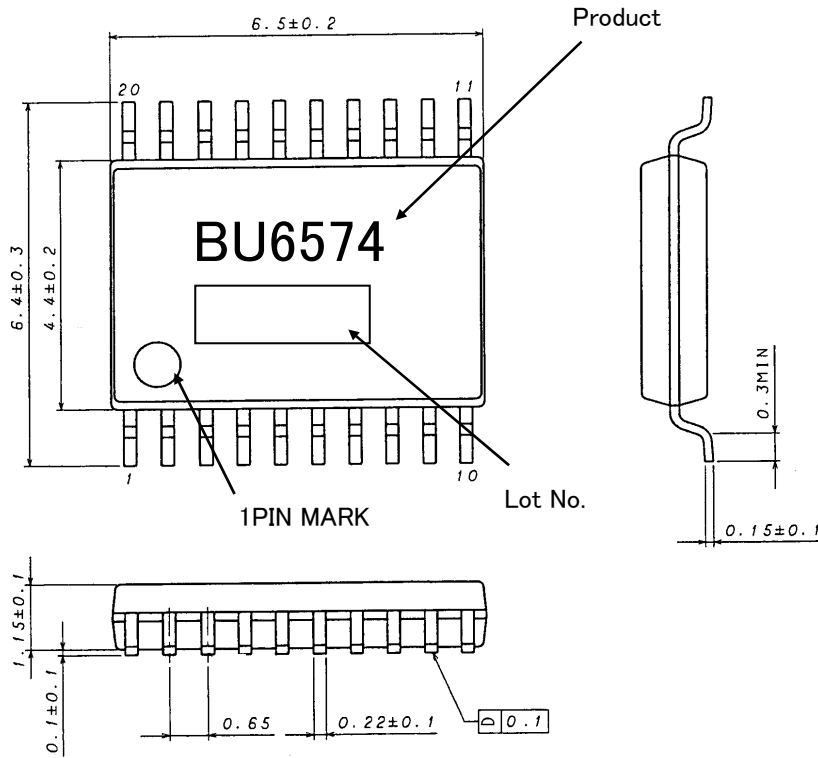
A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

◆Electrical characteristics (Unless otherwise noted, VAVDD=VDVDD=VVDDIO = 3.3V, Ta = 25°C)

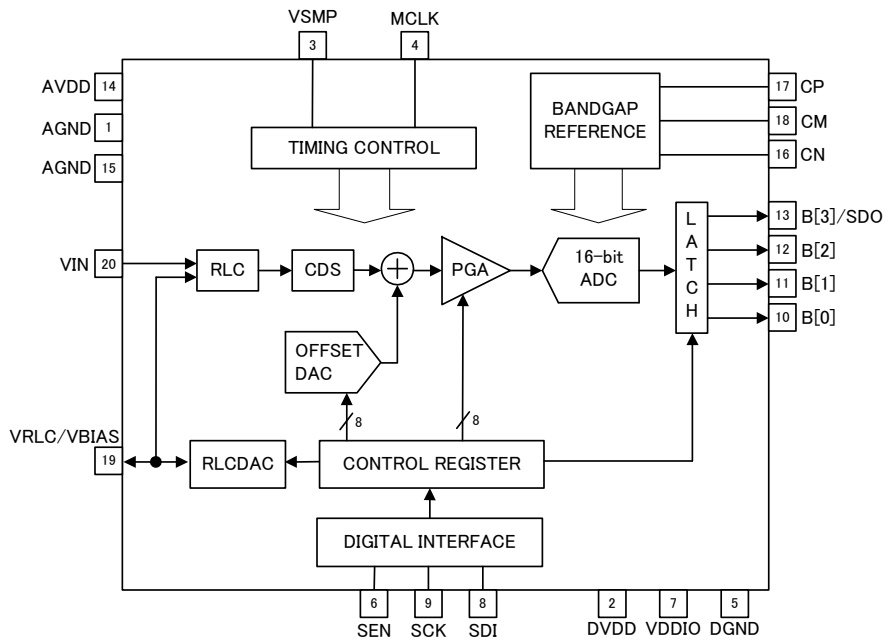
| Parameter | Symbol | MIN | TYP | MAX | Unit | Conditions |
|---|--------------------|-------------------------|--------------|------------------------|------|------------------------------|
| Overall System Specification | | | | | | |
| Input signal limits | V _{IN} | 0.26 | – | 2.7 | V | |
| Conversion Rate | RATE | – | – | 6 | MSPS | |
| Digital Inputs | | | | | | |
| High level input voltage | V _{IH} | 0.7*V _{VDDIO} | – | – | V | |
| Low level input voltage | V _{IL} | – | – | 0.2*V _{VDDIO} | V | |
| High level input current | I _{IH} | – | – | 1 | uA | |
| Low level input current | I _{IL} | – | – | 1 | uA | |
| Digital Outputs | | | | | | |
| High level output voltage | V _{OH} | V _{VDDIO} –0.5 | – | – | V | I _{OH} = 1mA |
| Low level output voltage | V _{OL} | – | – | 0.5 | V | I _{OL} = 1mA |
| Supply Currents | | | | | | |
| Total supply current - active | I _{TOTAL} | – | 35.7 41.7 | 70 | mA | MCLK = 12MHz MCLK = 24MHz |
| Total Analog AVDD, Supply current - active | I _{AVDD} | – | 32 34 | 50 | mA | MCLK = 12MHz MCLK = 24MHz |
| Total digital DVDD, Supply current - active | I _{DVDD} | – | 1.5 3.0 | 10 | mA | MCLK = 12MHz MCLK = 24MHz |
| Total digital I/O, Supply current - active | I _{VDDIO} | – | 2.2 4.4 | 10 | mA | MCLK = 12MHz MCLK = 24MHz |
| Supply current – full power down mode | I _{PD} | – | 30 | 60 | uA | MCLK=Low |

◆ Package outline



SSOP-B20 (Unit:mm)

◆ Block diagram



◆ Pin description

| Pin Number | Pin Name |
|------------|------------|
| 1 | AGND |
| 2 | DVDD |
| 3 | VSMP |
| 4 | MCLK |
| 5 | DGND |
| 6 | SEN |
| 7 | VDDIO |
| 8 | SDI |
| 9 | SCK |
| 10 | B[0] |
| 11 | B[1] |
| 12 | B[2] |
| 13 | B[3]/SDO |
| 14 | AVDD |
| 15 | AGND |
| 16 | CN |
| 17 | CP |
| 18 | CM |
| 19 | VRLC/VBIAS |
| 20 | VIN |

●Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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